

EAST SEARCH

1/27/2007

L#	Hits	Search String	Databases
S1	566094	(integrated or digital) near2 circuit\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	40	S1 and ((bus near2 (performance or traffic)) with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	1665	S1 and (bus with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	2232	S1 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	210	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	210	S2 or S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	23	S6 and (high near2 level near2 language\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	173	S6 and (source\$1 or algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	88	S6 and (source\$1 and algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	27	S6 and (bus with hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	156	S6 and (bus with data with transfer\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	8	S6 and (evaluation with function\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	11	S6 and (modif\$3 with source\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	1	S6 and ("general purpose" near2 language\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	60	S6 and (architecture with design)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	55	S11 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	24	S6 and (bus with process\$3 with rate\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	2	S6 and (bus with traffic\$3 with rate\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	132	S6 and (bus with traffic\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	11	S6 and (high near2 level near2 design\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	1	S6 and (performance with (feed\$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	1	S6 and ((evaluation or verification) with (feed\$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	24	S6 and (feed\$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	1	S6 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	103	S7 or S9 or S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	72	S12 or S13 or S16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	7	S17 and S19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	51	S17 or S20 or S23 or S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	3687	S3 or S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	10	S30 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	138	S25 or S26 or S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	566094	(integrated or digital) near2 circuit\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	40	S32 and ((bus near2 (performance or traffic)) with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	1665	S32 and (bus with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	2232	S32 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	210	S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	210	S33 or S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S38	8	S37 and (evaluation with function\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	10	S37 and (bus with "data transfer" with evaluation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	11	S37 and (high near2 level near2 design\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	11	S37 and (modif\$3 with source\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	24	S37 and (bus with process\$3 with rate\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	5	S37 and (bus with processing with rate\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	3687	S34 or S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	7	S44 and (bus with "processing rate")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	3	S44 and ("high level" near2 design\$1) with performance)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	55	S44 and ("high level" near2 design\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	24	S37 and (feed\$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	70	S44 and ((bus near2 performance) with (feedback\$3 or (feed near2 back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	943	S32 and (bus with simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	703	S50 and (source\$1 or (programming near2 language\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	168	S51 and (bus with (performance or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	83	S52 and (hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	403	S50 and (language\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	62	S53 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	1	S50 and ("bus traffic" with (count\$3 or increment\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	1	S50 and (bus with traffic with (count\$3 or increment\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	1	S50 and (bus with evaluation with increment\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	45	((integrated or digital) near2 circuit\$1) with ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	4890	((integrated or digital) near2 circuit\$1) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	5	((integrated or digital) near2 circuit\$1) with co-simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	17	((integrated or digital) near2 circuit\$1) same co-simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	4939	S59 or S60 or S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	56	S64 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	161	S64 and ((partit\$3 or allocat\$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	13	S64 and (bus near2 ((process\$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	40	S64 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	0	S64 and (profil\$3 with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	0	S64 and (profil\$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	117	S64 and (profil\$3 with (simulat\$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	4	S66 and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	333	S65 or S66 or S67 or S68 or S71 or S72	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	753	((integrated or digital) near2 circuit\$1) and ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	5612	S64 or S74	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S78	84	S75 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S79	228	S75 and ((partit\$3 or allocat\$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S80	31	S75 and (bus near2 ((process\$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S81	71	S75 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S82	0	S75 and (profil\$3 with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S83	1	S75 and (profil\$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S84	125	S75 and (profil\$3 with (simulat\$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S85	7	S79 and S84	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S86	446	S78 or S79 or S80 or S81 or S83 or S84 or S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S87	17	S75 and (profil\$3 with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S88	45	((integrated or digital) near2 circuit\$1) with ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S89	4890	((integrated or digital) near2 circuit\$1) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S90	17	((integrated or digital) near2 circuit\$1) same co-simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S91	4939	S88 or S89 or S90	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S92	753	((integrated or digital) near2 circuit\$1) and ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S93	5612	S91 or S92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S94	84	S93 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S95	228	S93 and ((partition\$3 or allocat\$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S96	31	S93 and (bus near2 ((process\$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S97	71	S93 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S98	1	S93 and (profil\$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S99	125	S93 and (profil\$3 with (simulat\$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	7	S95 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	446	S94 or S95 or S96 or S97 or S98 or S99 or S100	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	131	S93 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S103	726060	((integrated or digital) near2 circuit\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S104	51	S103 and ((bus near2 (performance or traffic)) with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S105	2194	S103 and (bus with (simulat\$3 or evaluat\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S106	3081	S103 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S107	277	S105 and S106	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S108	277	S104 or S107	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S109	201	S108 and ((configur\$3 or configuration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S110	5	S108 and ((modif\$3 or modification) with (configur\$3 or configuration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S111	17	S108 and ((reconfigur\$3 or reconfiguration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S112	55	S108 and ((bus or buss) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S113	0	S108 and ((modif\$3 or modification) with (bus or buss) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S114	0	S108 and ((modif\$3 or modification) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S115	25	S108 and ((modif\$3 or modification) with (bus or buss) with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S116	90	S110 or S111 or S112 or S115	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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Results of search set L29:S25 or S26 or S28

Document	Kind	Codes	Title
US 20050128489	A1		Parametric optimization of optical metrology model
US 20050122500	A1		System and method for lithography simulation
US 20050120327	A1		System and method for lithography simulation

Issue Date	Current OR	Abstract
20050616	356/601	
20050609	355/67	
20050602	716/20	

US 20050120012 A1	Adaptive hierarchy usage monitoring HVAC control system	20050602 707/3
US 20050108667 A1	METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVING MULTIPLE VOLTAGE DOMAINS	20050519 716/4
US 20050102125 A1	Inter-chip communication system	20050512 703/14
US 20050097500 A1	System and method for lithography simulation	20050505 716/20
US 20050094729 A1	System and hardware partitioning for multi-standard video compression and decompression	20050505 375/240.16
US 20050091633 A1	System and method for lithography simulation	20050428 716/20
US 20050086565 A1	System and method for generating a test case	20050421 714/741
US 20050081170 A1	Method and apparatus for accelerating the verification of application specific integrated circuit designs	20050414 716/6
US 20050081130 A1	Using constrained scan cells to test integrated circuits	20050414 714/726
US 20050076322 A1	System and method for lithography simulation	20050407 716/20
US 20050076282 A1	System and method for testing a circuit design	20050407 714/739
US 20050071706 A1	Slew rate control mechanism	20050331 713/503
US 20050065762 A1	ESD protection device modeling method and ESD simulation method	20050324 703/14
US 20050057748 A1	Selecting a hypothetical profile to use in optical metrology	20050317 356/237.5
US 20050042527 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20050224 430/5
US 20050039156 A1	Design method for essentially digital systems and components thereof and essentially digital systems	20050217 716/18
US 20050025054 A1	Extensible traffic generator for synthesis of network data traffic	20050203 370/235
US 20050015778 A1	Method and system for expressing the algorithms for the manipulation of hardware state using a method	20050120 719/321
US 20050004774 A1	Methods and systems for inspection of wafers and reticles using designer intent data	20050106 702/108
US 20040268278 A1	Managing power on integrated circuits using power islands	20041230 716/5
US 20040252701 A1	Systems, processes and integrated circuits for rate and/or diversity adaptation for packet communication	20041216 370/395.21
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209 713/330
US 20040249915 A1	Advanced multi-network client device for wideband multimedia access to private and public wireless networks	20041209 709/223
US 20040243959 A1	Design method for semiconductor integrated circuit device	20041202 716/7
US 20040236876 A1	Apparatus and method of memory access control for bus masters	20041125 710/22
US 20040236564 A1	Simulation of a PCI device's memory-mapped I/O registers	20041125 703/25
US 20040214150 A1	Interaction education system for teaching patient care	20041028 434/273
US 20040209169 A1	Method of Verifying the Placement of Sub-Resolution Assist Features in a Photomask Layout	20041021 430/5
US 20040204928 A1	Simulator apparatus and related technology	20041014 703/13
US 20040193957 A1	Emulation devices, systems and methods utilizing state machines	20040930 714/30
US 20040193390 A1	Method and apparatus for rapid evaluation of component mismatch in integrated circuit performance	20040930 703/2
US 20040193388 A1	Design time validation of systems	20040930 703/1
US 20040168044 A1	Input pipeline registers for a node in an adaptive computing engine	20040826 712/220
US 20040153301 A1	Integrated circuit development methodology	20040805 703/14
US 20040148151 A1	Model simulation and calibration	20040729 703/22
US 20040145033 A1	Integrated circuit devices and methods and apparatuses for designing integrated circuit devices	20040729 257/659
US 20040136587 A1	Method and device for determining the properties of an integrated circuit	20040715 382/145
US 20040131267 A1	Method and apparatus for performing quality video compression and motion estimation	20040708 382/236
US 20040124874 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20040701 326/30
US 20040123256 A1	Software traffic generator/analyser	20040624 716/4
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617 716/18
US 20040098687 A1	System and method for implementing a flexible top level scan architecture using a partitioning algorithm	20040520 716/7
US 20040088598 A1	Deskew architecture	20040506 713/503
US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analysis	20040422 716/8

US 20040054510 A1	System and method for simulating human movement	20040318 703/6
US 20040017575 A1	Optimized model and parameter selection for optical metrology	20040129 356/625
US 20040017574 A1	Model and parameter selection for optical metrology	20040129 356/625
US 20040010650 A1	Configurable multi-port multi-protocol network interface to support packet processing	20040115 710/305
US 20040004216 A1	Test assembly including a test die for testing a semiconductor product die	20040108 257/48
US 20040003362 A1	Timing abstraction and partitioning strategy	20040101 716/6
US 20030229877 A1	System and method for configuring analog elements in a configurable hardware device	20031211 716/16
US 20030229482 A1	Apparatus and method for managing integrated circuit designs	20031211 703/14
US 20030226062 A1	System and method for testing response to asynchronous system errors	20031204 714/38
US 20030225535 A1	Selection of wavelengths for integrated circuit optical metrology	20031204 702/76
US 20030216901 A1	Design apparatus and a method for generating an implementable description of a digital system	20031120 703/13
US 20030214326 A1	Distributed dynamically optimizable processing communications and storage system	20031120 326/101
US 20030212538 A1	Method for full-chip vectorless dynamic IR and timing impact analysis in IC designs	20031113 703/14
US 20030208728 A1	Method and system for simulating resist and etch edges	20031106 716/4
US 20030208350 A1	Facilitating simulation of a model within a distributed environment	20031106 703/22
US 20030204389 A1	Method for numerically simulating an electrical circuit	20031030 703/19
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023 712/229
US 20030200073 A1	Partitioning a model into a plurality of independent partitions to be processed within a distributed	20031023 703/17
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016 714/34
US 20030192029 A1	System and method for software development	20031009 717/101
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002 717/141
US 20030187853 A1	Distributed data storage system and method	20031002 707/10
US 20030187840 A1	Metrology diffraction signal adaptation for tool-to-tool matching	20031002 707/4
US 20030187602 A1	METROLOGY HARDWARE SPECIFICATION USING A HARDWARE SIMULATOR	20031002 702/94
US 20030163295 A1	Generation and use of integrated circuit profile-based simulation information	20030828 703/14
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807 716/18
US 20030144828 A1	Hub array system and method	20030731 703/21
US 20030142819 A1	Device and method for evaluating algorithms	20030731 380/28
US 20030142726 A1	Universal rake receiver	20030731 375/146
US 20030139956 A1	Methods and systems for role analysis	20030724 705/7
US 20030128140 A1	Code compression algorithms and architectures for embedded systems	20030710 341/107
US 20030126059 A1	Intellectual property (IP) brokering system and method	20030703 705/36R
US 20030125923 A1	Simulation of di/dt-induced power supply voltage variation	20030703 703/20
US 20030125922 A1	Mechanism for estimating and controlling di/dt-induced power supply voltage variations	20030703 703/18
US 20030093764 A1	Automated system-on-chip integrated circuit design verification system	20030515 716/5
US 20030093255 A1	Hot plug and hot pull system simulation	20030515 703/13
US 20030093252 A1	Message packet logging in a distributed simulation system	20030515 703/13
US 20030088840 A1	Method of designing semiconductor integrated circuit device, method of analyzing power consum	20030508 716/7
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424 716/8
US 20030079132 A1	Computer functional architecture and a locked down environment in a client-server architecture	20030424 713/182
US 20030075765 A1	Semiconductor integrated circuit	20030424 257/393
US 20030073060 A1	Interactive education system for teaching patient care	20030417 434/262
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220 716/4
US 20030018461 A1	Simulation monitors based on temporal formulas	20030123 703/14

US 20030016461 A1	Systems, apparatus, and methods to determine thermal decay characterization from an equalize	20030123 360/25
US 20030013024 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20030116 430/5
US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit design	20030109 716/6
US 20030008222 A1	Phase shift mask layout process for patterns including intersecting line segments	20030109 430/5
US 20030005263 A1	Shared resource queue for simultaneous multithreaded processing	20030102 712/218
US 20020197546 A1	Phase shift masking for "double-T" intersecting lines	20021226 430/5
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219 716/1
US 20020186721 A1	Methods and systems for monitoring traffic received from and loading simulated traffic on broadband	20021212 370/522
US 20020152060 A1	Inter-chip communication system	20021017 703/17
US 20020149598 A1	Method and apparatus for adjusting subpixel intensity values based upon luminance characteristics	20021017 345/589
US 20020147875 A1	Response and data phases in a highly pipelined bus architecture	20021010 710/305
US 20020144247 A1	System and apparatus for simultaneous optimization of code targeting multiple machines	20021003 717/155
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